Memory Compiler Notes for Special Pins

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| Date | Version | Comment | Author |
| 2016/12/28 | v1.0 | Initial version | Yi Li |
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1. **TEST1**

TEST1: TEST enable signal. This signal is for DFT team. Please tie TEST1 to 1'b0.

1. **RM/RME**

RME: Read Margin Enable. This signal control RM[2:0] whether select external input or internal default value.

RM[3:0]: Read Margin signal. RM[3:2] are synopsys test mode option. RM[1:0] are performance/yield option. 00:VDDMIN, 01:SLOW, 10:DEFAULT, 11:FAST.

There are 2 connection modes for different application.

**Case 1 :** Some design will run faster than its signoff frequency. (e.g. A7 signoff frequency 1.2GHz but will run at 2GHz in some case. ) For those design, we strongly suggest the following connection relationship table,

|  |  |
| --- | --- |
| RME | Register\* (default: 1'b0) |
| RM[3] | fixed value: 1'b0 |
| RM[2] | fixed value: 1'b0 |
| RM[1] | Register (default: 1'b1) |
| RM[0] | Register (default: 1'b0) |

Register\*: These pins will be tied to global registers. Generally, we can classify memory IPs into small/medium/large memory or write/read. One type memory could be connected one set of registers. For these register paths, we usually use constraints such as "set case 1/0 " or "set\_multiple\_cycle " in sdc file.

**Case 2:** Some design will only run at its signoff frequency. For those design, we suggest the following connection relationship table,

|  |  |
| --- | --- |
| RME | fixed value: 1'b0 |
| RM[3] | fixed value: 1'b0 |
| RM[2] | fixed value: 1'b0 |
| RM[1] | fixed value: 1'b1 |
| RM[0] | fixed value: 1'b0 |

1. **LS**

LS: Light Sleep signal for memory. High is available.

There are 3 connection strategies for our memory.

**Strategy 1:** For those memory don't need power gating function. Please tie this pin to fixed value 1'b0.

**Strategy 2:** For those timing can meet timing requirements. We can use memory enable signal ME to generate LS. That is

assign LS = ~ME

Note that LS should be inverted from ME.

**Strategy 3:** For those timing could not meet timing requirements by using ME signal. We should add global register into our design. These global register will be external input for LS pin. For these register paths, we usually use constraints such as "set case 1/0 " or "set\_multiple\_cycle " in sdc file.